UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
FRANKLIN, RICHARD B

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/737,191	MYLLY ET AL.
	Examiner	**Art Unit**	
	Richard Franklin	2181	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>17 October 2007</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-4,6-11,13,14 and 16-20</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-4,6-11,13,14 and 16-20</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1 – 4, 6 – 11, 13 – 14, and 16 – 20 are pending.

Continued Examination Under 37 CFR 1.114

2.   A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 17 October 2007 has been entered.

Response to Arguments

3.   Applicant's arguments with respect to claims 1 – 4, 6 – 11, 13 – 14, and 16 – 20 have been considered but are moot in view of the new ground(s) of rejection. The subject matter indicated as allowable in the Final Office Action mailed on 27 July 2007 has been removed by applicant in order remedy the rejection under 35 USC 112 1st Paragraph. Therefore, the notice of Allowable Subject Matter presented in the Final Office Action mailed on 27 July 2007 has been rescinded.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form

the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by
another filed in the United States before the invention by the applicant for patent or (2) a patent
granted on an application for patent by another filed in the United States before the invention by the
applicant for patent, except that an international application filed under the treaty defined in section
351(a) shall have the effects for purposes of this subsection of an application filed in the United States
only if the international application designated the United States and was published under Article 21(2)
of such treaty in the English language.

4.   Claims 1 – 3, 11, 13 – 14, and 17 – 20 are rejected under 35 U.S.C. 102(e) as

being anticipated by US Patent Application Publication No. 2003/0212857 (hereinafter

Pacheco).

As per claim 1, Pacheco teaches a method comprising transmitting information

(Figure 5B "BYTE 4-5 and 6-7") indicative of a time required for an initialization of a

respective one of at least two peripheral devices (Figure 2 Items 222, and 226a – 226n)

from each of the at least two peripheral devices (Paragraph [0040] Lines 12 – 15);

electrically combining the information from each of the at least two peripheral devices to

produce combined information indicating a time which is required at the most by any of

the at least two peripheral devices for its respective initialization (Figure 8A "Max Spin-

Up Period", Paragraph [0047] Lines 4 – 7); and using the combined information for

determining when at least one of the at least two peripheral devices is ready for

operation after completion of an initialization of each of the at least two peripheral

devices (Paragraph [0049] Lines 25 – 28 [Based on the startup times, the system

determines when a group of drives has spun-up and is initialized and is ready to move onto the next group of drives]).

As per claim 2, Pacheco also teaches wherein the information indicative of the time required for the initialization of the respective one of the at least two peripheral devices is an information indicative of the time required for the initialization of the respective one of the at least two peripheral devices at a maximum under regular circumstances (Figure 5B "BYTE 4-5, Typical Start Time (ms)", Paragraph [0034] Lines 7 – 9).

As per claim 3, Pacheco also teaches wherein at least one of the at least two peripheral devices transmits the information to the host device upon a predetermined command received from the host device (Figure 5A Item 500, Paragraph [0040] and Paragraph [0044] Lines 12 – 24).

As per claim 11, Pacheco teaches a bus (Figure 2 Item 202) configured to receive from at least two peripheral devices (Figure 2 Items 226a – 226n) an information indicative of a time required at a respective one of the at least two peripheral devices for its respective initialization (Figure 5B "BYTE 4-5 and 6-7") and configured to electrically combine the information to produce combined information indicating a time which is required at the most by any of the at least two peripheral devices for its respective initialization (Figure 8A "Max Spin-Up Period", Paragraph

[0047] Lines 4 – 7); an interface (Figure 2 Item 214) configured to interact with the at

least two peripheral devices via the bus; and a control component (Figure 2 Item 216)

configured to receive the combined information via the interface from the bus and to use

the combined information for determining when at least one of the at least two

peripheral devices is ready for operation after completion of an initialization of each of

the at least two peripheral devices (Paragraph [0049] Lines 25 – 28 [Based on the

startup times, the system determines when a group of drives has spun-up and is

initialized and is ready to move onto the next group of drives]).

As per claim 13, Pacheco teaches a system comprising a host device (Figure 2

Item 212) and at least two peripheral devices (Figure 2 Items 226a – 226n), each of the

at least two peripheral devices including: a first interface configured to interact with the

host device (The peripherals are described as SCSI drives and SCSI drives have SCSI

interfaces); a storing component configured to store information indicative of a time

required at a respective peripheral device for a respective initialization (Figure 2 Items

228a – 228n, Figure 5B "BYTE 4-5 and 6-7", Paragraph [0033] Lines 1 – 6, Paragraph

[0035]); and a controlling component (Paragraph [0035] "local disk drive controller")

configured to retrieve information indicative of the time required at the respective

peripheral device for the respective initialization from the storing component and

configured to transmit the information via the first interface to the host device; and the

host device including: a bus (Figure 2 Item 202) configured to receive from the at least

two peripheral devices the information indicative of the time required at the respective

peripheral device for its respective initialization and configured to electrically combine

the information to produce combined information indicating a time which is required at

the most by any of the at least two peripheral devices for its respective initialization

(Figure 8A "Max Spin-Up Period", Paragraph [0047] Lines 4 – 7); a second interface

(Figure 2 Item 214) configured to interact with the at least two peripheral devices via the

bus; and a control component (Figure 2 Item 216) configured to receive the combined

information via the second interface from the bus and to use the combined information

for determining when at least one of the at least two peripheral devices is ready for

operation after completion of an initialization of each of the at least two peripheral

devices (Paragraph [0049] Lines 25 – 28 [Based on the startup times, the system

determines when a group of drives has spun-up and is initialized and is ready to move

onto the next group of drives]).

As per claim 14, Pacheco teaches a computer program product comprising a

computer readable storage structure embodying computer program code thereon for

execution by a computer processor, wherein the computer program code comprises

instructions for performing a method comprising: receiving combined information

indicating a time which is required at the most be any of at least two peripheral devices

(Figure 2 Items 226a – 226n) for its respective initialization (Figure 8A "Max Spin-Up

Period", Paragraph [0047] Lines 4 – 7); and using the combined information for

determining when at least one of the at least two peripheral devices is ready for

operation after completion of an initialization of each of the at least two peripheral

devices (Paragraph [0049] Lines 25 – 28 [Based on the startup times, the system

determines when a group of drives has spun-up and is initialized and is ready to move

onto the next group of drives]).

As per claims 17 and 19, Pacheco teaches an apparatus comprising a bus

(Figure 2 Item 202) configured to electrically combine information indicative of a time

required for an initialization of a respective one of at least two peripheral devices (Figure

2 Items 226a – 226n) from each of the at least two peripheral devices to produce

combined information indicating a time which is required at the most be any of the at

least two peripheral devices for its respective initialization (Figure 8A "Max Spin-Up

Period", Paragraph [0047] Lines 4 – 7); and a control component (Figure 2 Item 216)

configured to use the combined information for determining when at least one of the at

least two peripheral devices is ready for operation after completion of an initialization of

each of the at least two peripheral devices (Paragraph [0049] Lines 25 – 28 [Based on

the startup times, the system determines when a group of drives has spun-up and is

initialized and is ready to move onto the next group of drives]).

As per claims 18 and 20, Pacheco also teaches a control module configured to

provide a predetermined command for transmission to at least one of the at least two

peripheral devices (Paragraph [0044] Lines 12 – 24).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over US

Patent Application Publication No. 2003/0212857 (hereinafter Pacheco) in view of US

Patent No. 5,566,351 (hereinafter Crittenden).

As per claim 4, Pacheco teaches the method as described per claim 1 (See

rejection of claim 1 above).

Pacheco does not teach wherein the host device uses the common initialization

timeout value for adapting a polling frequency which is to be employed for polling the at

least one of the at least two peripheral devices on whether the at least one peripheral

device has completed its respective initialization.

However, Crittenden teaches wherein the host device uses the uses the common

initialization timeout value for adapting a polling frequency which is to be employed for

polling the at least one of the at least two peripheral devices on whether the at least one

peripheral device has completed its respective initialization (Crittenden; Col 5 Lines 14 –

21).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to gave modified the teachings of Pacheco to include the

adaptive polling frequency because doing so allows for the system to maximize data

throughput by not permitting excessive sleep periods and simultaneously minimize

central processing (CPU) load by avoiding excessive polling (Crittenden; Col 5 Lines 26

– 29).

6.   Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over US

Patent Application Publication No. 2003/0212857 (hereinafter Pacheco) in view of US

Patent No. 6,964,018 (hereinafter Masui).

As per claim 6, Pacheco teaches the method as described per claim 1 using

SCSI devices (See rejection of claim 1 above).

Pacheco does not teach wherein one of the peripheral devices is a memory card.

However, Masui teaches wherein a SCSI device could be a memory card (Masui;

Col 13 Lines 41 – 44).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to have modified the teachings of Pacheco to include the

memory card because memory cards are an example of a storage device that can be

connected to a SCSI bus (Masui; Col 13 Lines 41 – 44).

7.   Claims 7 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over

US Patent Application Publication No. 2003/0212857 (hereinafter Pacheco) in view of

US Patent No. 6,964,018 (hereinafter Masui) and further in view of The MultiMediaCard

System Specification Version 3.31 by the MMCA Technical Committee (hereinafter

MMCA).

As per claims 7 – 10, Pacheco in combination with Masui teach the use of the method of claim 1 with a memory card.

Pacheco in combination with Masui does not teach wherein the memory card is a MultiMediaCard™ (MMC) system or implements MMC functions.

However, MMCA teaches the use of a MMC as a storage device (MMCA; Page 11 Paragraph 1); the peripheral devices transmit the information to the host device upon receipt of a CMD1 command from the host device (MMCA; Page 81 Section 6.3 Power Up); the peripheral devices retrieve the information from an operating condition register (OCR) of the peripheral devices (MMCA; Page 67 Section 5.1 OCR Register); and the peripheral devices transmit the information in an R3 response to the host device (MMCA; Pages 53 – 55 Section 4.9 Responses).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings Pacheco in combination with Masui because the use of the MMC system allows for low costs data storage that covers a large area of applications (MMCA; Page 11 Paragraph 1).

8.   Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2003/0212857 (hereinafter Pacheco) in view of US Patent No. 6,233,625 (hereinafter Vander Kamp).

As per claim 16, Pacheco teaches the method as described per claim 1 using SCSI devices and a SCSI bus (See rejection of claim 1 above)

Pacheco does not explicitly teach wherein transmitting information indicative of the time required for an initialization of a respective one of the at least two peripheral devices from each of the at least two peripheral devices via a bus to the host device is performed in an open drain mode of the bus.

However, Vander Kamp teaches that SCSI devices operate according to the SCSI-I or SCSI-II bus protocols (Vander Kamp; Col 5 Lines 39 – 40). The SCSI-I bus protocol is an open drain mode bus protocol.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings Pacheco to include the open drain mode because doing so is well known when using SCSI devices (Vander Kamp; Col 5 Lines 39 – 40).
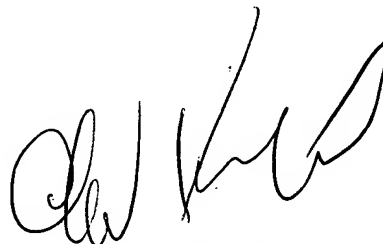
Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Richard Franklin whose telephone number is (571) 272-

0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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SUPERVISORY PATENT EXAMINER